Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

    1. (Previously Presented) A phase locked loop, comprising:

        a phase comparator having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

        a loop filter having an input for receiving the error signal and an output for providing a control signal;

        an oscillator having an input for receiving the control signal and an output for providing a timing signal, wherein the feedback signal is derived from the timing signal;

        a processor coupled to the oscillator, wherein the processor is further coupled to receive a status message indicative of a quality level of the reference clock signal; and

        a machine-readable medium coupled to the processor, wherein the machine-readable medium has instructions stored thereon capable of causing the processor to monitor the status message and to selectively place the phase locked loop in a holdover condition in response to the status message;

        wherein the instructions stored on the machine-readable medium are capable of causing the processor to place the phase locked loop in the holdover condition when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition.

2. (Original) The phase locked loop of claim 1, wherein the instructions stored on the machine-readable medium are capable of causing the processor to selectively place the phase locked loop in the holdover condition in response to the status message regardless of a validity of the reference clock signal.

3. (Canceled)

4. (Previously Presented) A phase locked loop, comprising:

a phase comparator having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal, wherein the reference clock signal is selected from a group consisting of a primary reference clock signal and at least one secondary reference clock signal;

a loop filter having an input for receiving the error signal and an output for providing a control signal;

an oscillator having an input for receiving the control signal and an output for providing a timing signal, wherein the feedback signal is derived from the timing signal;

a processor coupled to the oscillator, wherein the processor is further coupled to receive status messages indicative of a quality level of the primary reference clock signal and the at least one secondary reference clock signal; and

a machine-readable medium coupled to the processor, wherein the machine-readable medium has instructions stored thereon capable of causing the processor to monitor the status messages and to selectively

place the phase locked loop in a holdover condition in response to the

status messages;

wherein the instructions stored on the machine-readable medium are capable of

causing the processor to place the phase locked loop in the holdover

condition when a quality level of the primary reference clock signal and

the at least one secondary reference clock signal indicated by the status

message is less than an expected quality level of the phase locked loop in

the holdover condition.

5. (Previously Presented) A phase locked loop, comprising:

a phase comparator having a first input for receiving a reference clock signal, a

second input for receiving a feedback signal, and an output for providing

an error signal;

a loop filter having an input for receiving the error signal and an output for

providing a control signal;

an oscillator having an input for receiving the control signal and an output for

providing a timing signal, wherein the feedback signal is derived from the

timing signal;

a processor coupled to the oscillator, wherein the processor is further coupled to

receive a status message indicative of a quality level of the reference clock

signal; and

a machine-readable medium coupled to the processor, wherein the

machine-readable medium has instructions stored thereon capable of

causing the processor to monitor the status message and to place the phase

locked loop in a holdover condition if the quality level indicated by the

status message is below a target quality level;

wherein the target quality level is an expected quality level of the phase locked

loop in the holdover condition.

6. (Canceled)

7. (Original) The phase locked loop of claim 5, wherein the expected quality level is at

least a Stratum 2 level.

8. (Original) The phase locked loop of claim 5, wherein the instructions stored on the

machine-readable medium are capable of causing the processor to monitor the

status message and to place the phase locked loop in the holdover condition if the

quality level indicated by the status message is below the target quality level when

the reference clock signal is valid.

9. (Previously Presented) A phase locked loop, comprising:

a phase comparator having a first input for receiving a reference clock signal, a

second input for receiving a feedback signal, and an output for providing

an error signal, wherein the reference clock signal is selected from a group

consisting of a primary reference clock signal and at least one secondary

reference clock signal;

a loop filter having an input for receiving the error signal and an output for

providing a control signal;

an oscillator having an input for receiving the control signal and an output for

providing a timing signal, wherein the feedback signal is derived from the

timing signal;

a processor coupled to the oscillator, wherein the processor is further coupled to

receive status messages indicative of a quality level of the primary

reference clock signal and the at least one secondary reference clock

signal; and

a machine-readable medium coupled to the processor, wherein the

machine-readable medium has instructions stored thereon capable of

causing the processor to monitor the status messages and to place the

phase locked loop in a holdover condition if the quality level indicated by

each status message is below a target quality level regardless of a validity

of any reference clock signal;

wherein the target quality level is an expected quality level of the phase locked

loop in the holdover condition.

10. (Previously Presented) A timing circuit, comprising:

a receiver coupled to receive a communications signal and for recovering clock

and data signals and a status message therefrom;

a framer for locating a frame pulse and generating a reference clock signal from

the recovered clock and data signals; and

a phase locked loop coupled to receive the reference clock signal and to generate

a timing signal therefrom, the phase locked loop comprising:

a phase comparator having a first input for receiving a reference clock

signal, a second input for receiving a feedback signal, and an

output for providing an error signal;

a loop filter having an input for receiving the error signal and an output

for providing a control signal;

an oscillator having an input for receiving the control signal and an

output for providing a timing signal, wherein the feedback signal

is derived from the timing signal;

a processor coupled to the oscillator, wherein the processor is further

coupled to receive the status message, wherein the status message

is indicative of a quality level of the reference clock signal; and

a machine-readable medium coupled to the processor, wherein the

machine-readable medium has instructions stored thereon capable

of causing the processor to monitor the status message and to

selectively place the phase locked loop in a holdover condition in

response to the status message; and

a pre-scaler interposed between the framer and the phase locked loop.

11. (Canceled)

12. (Previously Presented) A timing circuit, comprising:

a receiver coupled to receive a communications signal and for recovering clock

and data signals and a status message therefrom;

a framer for locating a frame pulse and generating a reference clock signal from

the recovered clock and data signals; and

a phase locked loop coupled to receive the reference clock signal and to generate

a timing signal therefrom, the phase locked loop comprising:

a phase comparator having a first input for receiving a reference clock

signal, a second input for receiving a feedback signal, and an

output for providing an error signal;

a loop filter having an input for receiving the error signal and an output

for providing a control signal;

an oscillator having an input for receiving the control signal and an output

for providing a timing signal, wherein the feedback signal

is derived from the timing signal;

a processor coupled to the oscillator, wherein the processor is further

coupled to receive the status message, wherein the status message

is indicative of a quality level of the reference clock signal; and

a machine-readable medium coupled to the processor, wherein the

machine-readable medium has instructions stored thereon capable

of causing the processor to monitor the status message and to

place the phase locked loop in a holdover condition if the quality

level indicated by the status message is below a target quality level;

and

a pre-scaler interposed between the framer and the phase locked loop.

13.(Original) The timing circuit of claim 12, wherein the instructions stored on the

machine-readable medium are capable of causing the processor to monitor the

status message and to place the phase locked loop in the holdover condition if the

quality level indicated by the status message is below the target quality level when

the reference clock signal is valid.

14. (Cancelled)

15. (Previously Presented) A shelf controller for controlling synchronization of shelf

elements in a communications network element, the shelf controller comprising:

a processor;

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a machine-readable medium coupled to the processor; and

a timing circuit coupled to the processor and providing a timing signal for
controlling synchronization of the shelf elements in the communications
network element, wherein the timing circuit comprises:

a receiver coupled to receive a communications signal and for
recovering clock and data signals and a status message
therefrom;

a framer for locating a frame pulse and generating a reference clock
signal from the recovered clock and data signals, wherein
the

status message is indicative of a quality level of the reference clock
signal; and

a phase locked loop coupled to receive the reference clock signal
and to generate a timing signal therefrom, the phase locked
loop comprising:

a phase comparator having a first input for receiving
a reference

clock signal, a second input for receiving a feedback

signal, and an output for providing an error signal;

a loop filter having an input for receiving the error
signal and an output for providing a control
signal; and

an oscillator coupled to the processor and having an
input for receiving the control signal and an
output for providing a timing signal, wherein

the feedback signal is derived from the

timing signal;

wherein the machine-readable medium has instructions stored thereon capable of

causing the processor to monitor the status message and to selectively

place the phase locked loop in a holdover condition in response to the

status message; and

wherein the instructions stored on the machine-readable medium are capable of

causing the processor to place the phase locked loop in the holdover

condition when a quality level of the reference clock signal indicated by

the status message is less than an expected quality level of the phase

locked loop in the holdover condition .

16. (Original) A network element for a communications network, the network element

comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality

of shelf elements includes at least one shelf controller for controlling

synchronization of the plurality of shelf elements, the at least one shelf

controller comprising:

a processor;

a machine-readable medium coupled to the processor; and

a timing circuit coupled to the processor and providing a timing

signal for controlling synchronization of the shelf elements in

the communications network element, wherein the timing

circuit comprises:

a receiver coupled to receive a communications signal and
for recovering clock and data signals and a status
message therefrom;

a framer for locating a frame pulse and generating a
reference clock signal from the recovered clock and
data signals, wherein the status message is
indicative of a quality level of the reference clock
signal; and

a phase locked loop coupled to receive the reference clock
signal and to generate a timing signal therefrom, the
phase locked loop comprising:

a phase comparator having a first input for
receiving a reference clock signal, a
second input for receiving a feedback
signal, and an output for providing
an error signal;

a loop filter having an input for receiving the
error signal and an output for
providing a control signal; and

an oscillator coupled to the processor and
having an input for receiving the
control signal and an output for
providing a timing signal, wherein
the feedback signal is derived from
the timing signal;

wherein the timing circuit provides a synchronization timing signal to the shelf

backplane for the synchronization of the plurality of shelf elements;

wherein the synchronization timing signal is derived from the first timing signal;

and

wherein the machine-readable medium has instructions stored thereon capable of

causing the processor to monitor the status message and to selectively

place the phase locked loop in a holdover condition in response to the

status message.

17. (Currently Amended) A method of generating a timing signal, comprising:

generating the timing signal from a reference clock signal in a phase locked loop;

monitoring a status message indicative of a quality level of the reference clock

signal; and

placing the phase locked loop in a holdover condition if the quality level

indicated by the status message is below a target level;

wherein the method is performed in the order presented;

wherein the target level is an expected quality level of the phase locked loop in the

holdover condition.

18. (Canceled)

19. (Canceled)

20. (Currently Amended) The method of claim ~~19~~ 17, wherein the expected quality level is a Stratum 2 level.

21. (Original) The method of claim 17, wherein placing the phase locked loop in the holdover condition if the quality level indicated by the status message is below the target level occurs when the reference clock signal is valid.

22. (Previously Presented) A method of generating a timing signal, comprising:

generating the timing signal from a reference clock signal in a phase locked

loop, wherein the reference clock signal is selected from the group consisting of a primary reference clock signal and at least one secondary reference clock signal;

monitoring status messages indicative of a quality level of the primary reference clock signal and the at least one secondary reference clock signal; and

placing the phase locked loop in a holdover condition if the quality level

indicated by each status message is below a target level regardless of a validity of any reference clock signal; and

wherein the method is performed in the order presented.

23. (Canceled)

24. (Original) The method of claim 22, further comprising:

maintaining the phase locked loop in the holdover condition until at least one of

the reference clock signals is valid and has a status message indicating a quality

level at or above the target level.

25. (Original) The method of claim 24, wherein the phase locked loop is maintained in

the holdover condition for a predetermined period after a reference clock signal

having a valid status has a status message indicating a quality level at or above the

target level.

26. (Previously Presented) A method of generating a timing signal, comprising:

during a time when a primary reference clock signal is valid and has an indicated

quality level at or above a target level:

generating a first error signal indicative of a phase relationship

between the primary reference clock signal and a first

feedback signal;

filtering the first error signal to produce a first control signal;

generating the timing signal in response to the first control signal;

and

deriving the first feedback signal from the timing signal;

during a time when the primary reference clock signal is failed or has an indicated

quality level below the target level, and when a secondary reference clock

signal is valid and has an indicated quality level at or above the target

level:

generating a second error signal indicative of a phase relationship

between the secondary reference clock signal and a second

feedback signal;

filtering the second error signal to produce a second control signal;

generating the timing signal in response to the second control
signal; and

deriving the second feedback signal from the timing signal; and

during a time when each reference clock signal is failed or has an indicated
quality level below the target level:
generating a holdover control signal; and

generating a timing signal in response to the holdover control
signal;

wherein the method is performed in the order presented.

27. (Canceled)

28. (Previously Presented) A method of generating a timing signal, comprising:
during a time when a primary reference clock signal is valid and has an indicated
quality level at or above a target level:
generating a first error signal indicative of a phase relationship between
the primary reference clock signal and a first feedback signal;

filtering the first error signal to produce a first control signal;

generating the timing signal in response to the first control signal; and

deriving the first feedback signal from the timing signal;

during a time when the primary reference clock signal either is failed or is valid
and has an indicated quality level below the target level, and when a

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secondary reference clock signal is valid and has an indicated quality level at or above the target level:

>> generating a second error signal indicative of a phase relationship between the secondary reference clock signal and a second feedback signal;

>> filtering the second error signal to produce a second control signal;

>> generating the timing signal in response to the second control signal; and

>> deriving the second feedback signal from the timing signal; and

> during a time when each reference clock signal either is failed or is valid and has an indicated quality level below the target level:

> generating a holdover control signal; and

> generating a timing signal in response to the holdover control signal;

wherein the method is performed in the order presented.

29. (Canceled)

30. (Previously Presented) A machine-readable medium having instructions stored thereon capable of causing a processor to perform a method of generating a timing signal, the method comprising:

>> generating the timing signal from a reference clock signal in a phase locked loop;

> monitoring a status message indicative of a quality level of the reference clock signal; and

placing the phase locked loop in a holdover condition if the quality level

indicated by the status message is below a target level;

wherein the method is performed in the order presented.

31. (Original) The machine-readable medium of claim 30, wherein placing the phase

locked loop in the holdover condition if the quality level indicated by the status

message is below the target level occurs when the reference clock signal is valid.

32. (Previously Presented) A machine-readable medium having instructions stored

thereon capable of causing a processor to perform a method of generating a timing

signal, the method comprising:

generating the timing signal from a reference clock signal in a phase

locked loop, wherein the reference clock signal is selected from the

group consisting of a primary reference clock signal and at least

one secondary reference clock signal;

monitoring status messages indicative of a quality level of the primary

reference clock signal and the at least one secondary reference

clock signal; and

placing the phase locked loop in a holdover condition if the quality level

indicated by each status message is below a target level regardless

of a validity of any reference clock signal;

wherein the method is performed in the order presented.

33. (Previously Presented) A machine-readable medium having instructions stored
thereon capable of causing a processor to perform a method of generating a timing
signal, the method comprising:

during a time when a primary reference clock signal is valid and has an
indicated quality level at or above a target level:

generating a first error signal indicative of a phase
relationship between the primary reference clock
signal and a first feedback signal;

filtering the first error signal to produce a first control
signal;

generating the timing signal in response to the first control
signal; and

deriving the first feedback signal from the timing signal;

during a time when the primary reference clock signal is failed or has an
indicated quality level below the target level, and when a
secondary reference clock signal is valid and has an indicated
quality level at or above the target level:

generating a second error signal indicative of a phase
relationship

between the secondary reference clock signal and a second
feedback signal;

filtering the second error signal to produce a second control
signal;

generating the timing signal in response to the second
control signal; and

deriving the second feedback signal from the timing signal;

and

during a time when each reference clock signal is failed or has an indicated

quality level below the target level:

generating a holdover control signal; and

generating a timing signal in response to the holdover

control signal;

wherein the method is performed in the order presented.

34. (Previously Presented) A machine-readable medium having instructions stored

thereon capable of causing a processor to perform a method of generating a timing

signal, the method comprising:

during a time when a primary reference clock signal is valid and has an

indicated quality level at or above a target level:

generating a first error signal indicative of a phase relationship

between

the primary reference clock signal and a first feedback signal;

filtering the first error signal to produce a first control signal;

generating the timing signal in response to the first control signal;

and

deriving the first feedback signal from the timing signal;

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during a time when the primary reference clock signal either is failed or is

valid and has an indicated quality level below the target level, and

when a secondary reference clock signal is valid and has an

indicated quality level at or above the target level:

generating a second error signal indicative of a phase

relationship

between the secondary reference clock signal and a second

feedback signal;

filtering the second error signal to produce a second control

signal;

generating the timing signal in response to the second

control signal; and

deriving the second feedback signal from the timing signal;

and

during a time when each reference clock signal either is failed or is valid

and has an indicated quality level below the target level:

generating a holdover control signal; and

generating a timing signal in response to the holdover

control signal;

wherein the method is performed in the order presented.